WHAT IS CLAIMED IS:

1. A cache comprising:

a memory including a plurality of entries, wherein each of said plurality of entries is configured to store a cache line of data; and

a control circuit coupled to said memory, said control circuit configured to select a first entry of said plurality of entries for access responsive to a first transaction which explicitly specifies said first entry.

2. The cache as recited in claim 1 wherein said cache is set associative, and wherein said first transaction explicitly specifies a first index and a first way corresponding to said first entry.

3. The cache as recited in claim 2 wherein said first transaction includes a first address, and wherein said first address includes an index portion specifying said first index, and wherein said first address includes a way portion specifying said first way.

4. The cache as recited in claim 1, wherein said first transaction includes a first address, and wherein said first address is included in a first address space separate from a second address space corresponding to a memory system.

5. The cache as recited in claim 2 further comprising a replacement circuit configured to select a way for eviction in response to a cache miss, and wherein said replacement circuit is configured to select said first way for a subsequent cache miss responsive to said first transaction.

6. The cache as recited in claim 1 wherein said first transaction is a write transaction, and wherein said write transaction includes first data, and wherein said control circuit causes

said first data to be written to said first entry responsive to said write transaction.

7. The cache as recited in claim 6 wherein said first entry further includes a tag information, and wherein said control circuit causes a tag portion of a first address of said write transaction to be written to said tag information.

8. The cache as recited in claim 6 wherein said first entry further includes a tag information, and wherein said first address includes a first valid indication, and wherein said tag information includes a valid indication, and wherein said control circuit is configured to cause said first valid indication to be written to said valid indication of said tag information.

9. The cache as recited in claim 6 wherein said first entry further includes a tag information, and wherein said first address includes a first dirty indication, and wherein said tag information includes a dirty indication, and wherein said control circuit is configured to cause said first dirty indication to be written to said dirty indication of said tag information.

10. The cache as recited in claim 1 wherein said first transaction is a read transaction, and wherein said cache is configured to return first data from said first entry responsive to said read transaction.

11. The cache as recited in claim 1 further comprising a register coupled to receive a tag information from said first entry responsive to said first transaction.

12. The cache as recited in claim 11 wherein said control circuit is configured to cause a contents of said register to be returned in response to a second transaction targeting said register.

13. A system comprising:

a cache including a plurality of entries, wherein each of said plurality of entries is configured to store a cache line of data; and

a first circuit coupled to said cache, wherein said first circuit is configured to initiate a first transaction explicitly specifying a first entry of said plurality of entries;

wherein said cache is configured to select said first entry for access responsive to said first transaction.

14. The system as recited in claim 13 wherein said cache is set associative, and wherein said first transaction explicitly specifies a first index and a first way corresponding to said first entry.

15. The system as recited in claim 14 wherein said first transaction includes a first address, and wherein said first address includes an index portion specifying said first index, and wherein said first address includes a way portion specifying said first way.

16. The system as recited in claim 13 wherein said first transaction includes a first address, and wherein said first address is included in a first address space separate from a second address space corresponding to a memory system.

17. The system as recited in claim 13 wherein said circuit is a processor.

18. The system as recited in claim 13 wherein said circuit is an input/output (I/O) bridge, wherein said I/O bridge is configured to initiate said transaction on behalf of an I/O device coupled thereto.

19. A method for testing a cache, the method comprising:

performing a first transaction to cause first data to be stored in a first entry of a cache;

performing a read transaction explicitly specifying said first entry subsequent to performing said first transaction; and

comparing second data returned in response to said read transaction to said first data to detect if an error occurred in said first entry.

20. The method as recited in claim 19 wherein said first transaction is a write transaction explicitly specifying said first entry.

21. The method as recited in claim 19 wherein said first transaction is a memory transaction having an index of said first entry, the method further comprising:

performing a second transaction explicitly specifying said first entry prior to performing said first transaction; and

establishing said first entry as next to be replaced in response to said second transaction;

and wherein said performing said first transaction comprises:

detecting a miss in said cache for said first transaction; and

selecting said first entry to store said first data responsive to said establishing.

22. The method as recited in claim 19 further comprising storing a tag from said first entry in a register within said cache responsive to said read transaction.

23. The method as recited in claim 22 further comprising:

performing a second transaction to read said register; and

comparing said tag to a tag portion of a first address of said first transaction to

detect if an error occurred in said first entry.